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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,104	12/23/2003	Mitsuhiko Ogihara	MAE 305	8001

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,104	OGIHARA ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6,9,10,18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,6,9,10,18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/15/07 has been entered.

Response to Amendment

Amendment filed 3/15/07 with aforementioned Request for Continued Examination forms the basis for this Office Action. In said Amendment Applicants cancelled claims 3, 4, 16, 17, 19, 26-32 and 35-36. Claims 1, 7, 8, 11-15, 21-25, 33 and 34 previously had been cancelled. Accordingly, claims 2, 5, 6, 9, 10, 18 and 20 are in the application. Applicants substantially amended all pending claims through substantial amendment of independent claim 5. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Specification

The following is a quotation from the relevant sections of the Patent Rules under 37 C.F.R. 1.75 that form the basis of the objection made in this office action.

(d)

(1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (see § 1.58(a)).

1. Although the limitation that said semiconductor thin film is made of a compound semiconductor as a main material is disclosed in original claim 16, the remainder of the Specification should also disclose said limitation in exactly the same degree of broadness and specificity, for instance by amendment of the sentence on page 10, third paragraph, where applicants could overcome this objection by replacing "Further, the material of the LED epitaxial film 110 may be replaced by other material, such as...." by: "Further, the material of the LED epitaxial film 110 may be replaced by other material, e.g., a compound semiconductor, such as....".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 2, 5-6, 9-10 and 18*** are rejected under 35 U.S.C. 102(b) as being anticipated by Konuma et al (US 2001/0019133 A1).

On independent claim 5: Konuma et al teach a combined semiconductor apparatus ([0009]-[0024], [0043]-[0251] and Figures 1-14; specifically also title and abstract: both control of current and light-emitting components being comprised in said apparatus), comprising:

a silicon substrate 11/38 ([0044] for 11, [0013] for 38: note that i-Si is included in the embodiments of passivation film 38) having an integrated circuit formed therein (thin film transistors (TFTs) 201 and 202: see [0049]-[0057]), the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit (wiring pattern comprising source and drain electrodes 21, 22, 36 and 37 of said thin film transistors 201 and 202, e.g.);

a planarized region (the portion of 39 (see [0014]) within the lateral extent of EL device 203: see [0056]) defined over said rough or irregular surface of said silicon substrate;

a thin film (either 40 or 40/41a/41b (see [0063]-[0064] and [0068]-[0080]) disposed over said planarized region; and

a semiconductor thin film 42 (see [0081]-[0082]) disposed over said thin film (N.B.: the recited organic materials are semiconductors: see, e.g., col. 15, l. 8-25 in Yamazaki et al (6,739,931 B2), cited here not for teaching at least in this respect not, but merely for recitation of fact),

the semiconductor thin film including a light-emitting element 42 (loc.cit.) and being bonded on said thin film 40, so that said semiconductor thin film is disposed above the integrated circuit and said thin film 40 electrically connects said light-emitting element to said integrated circuit (because 40 is a pixel electrode connected to drain wiring 37 of TFT 202 as well as abutting the EL layer 42 according to its function as pixel electrode), wherein:

said semiconductor thin film is made of a compound semiconductor as a main material (the recited organic semiconductor materials are also compounds); and

a surface of said thin film 40 on a side of said semiconductor thin film is made as planar as possible (being the surface on which the EL layer 42 is formed) (see [0014]).

Therefore, said thin film 40 meets the limitation "planarized film" as well.

In this regard it is noted that the limitations "planarized" (claim 5, lines 6, 8 (twice), 9, 11, 13 and 17) and "has been subjected to a planarizing process" (final line of claim 5) constitute product-by-process limitations and are only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting the final structure, are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the relevant layers have been made to be as planar as possible (see above) and hence the limitations are met to the extent impacting on the final structure.

In conclusion, Konuma et al anticipate claim 5.

On claim 2: said planarized region formed by 39 is a part of said surface of said planarized silicon substrate 11/38 ([0061]). The limitation "which has been subjected to a planarizing process" constitutes a product-by-process limitation and hence is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting the final structure, are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, the relevant layer has been made to be planar and hence the limitations are met to the extent impacting on the final structure.

On claim 6: said planarized film includes an electrically conductive layer contacting with said light-emitting element (pixel electrode 40); and an inter-dielectric layer formed in a region peripheral to said electrically conductive layer (41a, 41b) (see [0068]-[0080]) (N.B.: protective layer 41 abuts pixel electrode 40, and hence the thin film may be defined to be 40/41a/41b, which is planarized in a sub-region, hence meets the limitation 'planarized film').

On claim 9: said semiconductor film 42 has a common electrode layer 43 on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor film (see common electrode 352 in Figure 12 and discussion, [0167], of an EL device with additional sealing structure but otherwise identical to the device of Figure 10, which is the device with pixel depicted in Figure 2, and hence element 352 is equivalent to electrode 43 therein), in which said light-emitting element is formed, and said second surface of said semiconductor thin film is disposed on a side (namely the upper side) of said planarized region of said silicon substrate.

On claim 10: said integrated circuit includes individual electrode terminals (source, drain electrode terminals and gate electrode terminals of both TFT 201 and TFT 202); and said apparatus further comprises individual interconnecting lines formed on a region extending from an upper surface of said light-emitting element to said individual terminals (see Figure 10, interconnecting lines 612, 613 and 614, e.g.: see [0154]).

On claim 18: said light-emitting elements are a plurality of light-emitting elements arranged in said semiconductor thin film (Figures 3A and 3B, see [0043]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claim 20*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Konuma et al as applied to claim 5, in view of Tsuruoka et al (JP 2001167874 A).

As detailed above, Konuma et al anticipate claim 5. Konuma et al do not necessarily teach the further limitation defined by claim 20. However, it would have been obvious to include said further limitation in view of Tsuruoka et al, who, in a patent document on an organic electroluminescent element, hence analogous art, teach the application of said organic electroluminescent element as the light source of an optical printer head (see English Abstract and also Derwent Abstract). Motivation to include the teaching by Tsuruoka et al in the invention by Konuma et al at least derives from the benefit of high picture quality and low manufacturing cost, as explicitly stated by Tsuruoka et al (see English Abstract, as well as 'Advantage' in Derwent Abstract).

Response to Arguments

Applicant's arguments filed 3/15/07 have been fully considered but they are not persuasive. Specifically, although the argument of traverse with regard to the claims as currently substantially amended is persuasive, an update search necessitates a rejection over Konuma et al (and Tsuruoka et al additionally for claim 20). Please note that unlike in Zhang the semiconductor thin film 42 in Konuma et al is indeed disposed above the integrated circuit formed by thin film transistors 201 and 202 (see Figure 2 and discussion).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
May 27, 2007

Primary Patent Examiner:
Johannes Mondt (TC3600, Art Unit: 3663)